L Number	Hits	Search Text	DB	Time stamp
1	99	wafer and chips and interposer and (coupling or attach$4) and dicing	USPAT; US-PGPUB	2002/06/03 14:52
2	85	(wafer and chips and interposer and (coupling or attach$4) and dicing) and (testing or performance or (leakage near2 current) or (offest adj voltage) or (gain adj tracking) or bandwidth)	USPAT; US-PGPUB	2002/06/03 14:54
3	59	((wafer and chips and interposer and (coupling or attach$4) and dicing) and (testing or performance or (leakage near2 current) or (offest adj voltage) or (gain adj tracking) or bandwidth)) and (chip with assembly)	USPAT; US-PGPUB	2002/06/03 14:55
4	51	(((wafer and chips and interposer and (coupling or attach$4) and dicing) and (testing or performance or (leakage near2 current) or (offest adj voltage) or (gain adj tracking) or bandwidth)) and (chip with assembly)) and @ad<=20001002	USPAT; US-PGPUB	2002/06/03 15:36
5	12	((((wafer and chips and interposer and (coupling or attach$4) and dicing) and (testing or performance or (leakage near2 current) or (offest adj voltage) or (gain adj tracking) or bandwidth)) and (chip with assembly)) and @ad<=20001002) and selecting	USPAT; US-PGPUB	2002/06/03 14:59
6	12	((((wafer and chips and interposer and (coupling or attach$4) and dicing) and (testing or performance or (leakage near2 current) or (offest adj voltage) or (gain adj tracking) or bandwidth)) and (chip with assembly)) and @ad<=20001002) and (selecting or sorting)	USPAT; US-PGPUB	2002/06/03 15:25
8	39	((((wafer and chips and interposer and (coupling or attach$4) and dicing) and (testing or performance or (leakage near2 current) or (offest adj voltage) or (gain adj tracking) or bandwidth)) and (chip with assembly)) and @ad<=20001002) not (((((wafer and chips and interposer and (coupling or attach$4) and dicing) and (testing or performance or (leakage near2 current) or (offest adj voltage) or (gain adj tracking) or bandwidth)) and (chip with assembly)) and @ad<=20001002) and selecting)	USPAT; US-PGPUB	2002/06/03 15:36

DOCUMENT-IDENTIFIER: US 5672980 A
TITLE: Method and apparatus for **testing** integrated circuit chips

---------- KWIC ---------

TTL:
Method and apparatus for **testing** integrated circuit chips

ABPL:
A method and apparatus for **testing** semi-conductor chips is disclosed. The individual semiconductor chips have I/O contacts. The apparatus is provided with an **interposer** that has contacts corresponding to the contacts on the semiconductor chip. Both the chip and the **interposer** contacts can be any known type including metal ball, bumps, or tabs or may be provided with dendritic surfaces. The chip contacts are first brought into relative loose temporary contact with the contacts on the **interposer** and then a compressive force greater that 5 grams per chip contact is applied to the chip to force the chip contacts into good electrical contact with the **interposer** contacts. **Testing** of the chip is then performed. The tests may include heating of the chip as well as the application of signals to the chip contacts. After **testing** the chip is removed from the substrate.

BSPR:
The invention relates to integrated circuit chip **testing**. More particularly, the invention relates to a method and apparatus for **testing** individual semiconductor chips before they are permanently **attached** to a chip carrier, printed circuit card or the like.

BSPR:

In the population of integrated circuit chip carriers, including thermally conductive modules, ceramic substrates, and polymeric substrates, it is necessary to minimize the shipment of modules with defective integrated circuit chips, while minimizing the cost of **testing** and replacement.

BSPR:
Integrated circuit chips are subjected to various **wafer** level tests during various stages of fabrication prior to **dicing**. However, after **dicing** it is particularly difficult and expensive to test integrated circuit chips. One reason is that an integrated circuit chip must be tested through its pins and contacts or pads before populating of the carrier, card, board, or the like.

BSPR:
Typically, integrated circuit **chips are attached** to a chip carrier, thermally conductive module chip carrier, circuit card or board, e.g., by solder bonding, brazing, controlled collapse chip connect, wire lead bonding, metal bump bonding, tape automated bonding, or the like.

BSPR:
The chip is then tested as part of an assembly and when a fault is found, the chip is removed from the card or board. This is not a simple "desoldering" step, especially in the case of high I/O density chips, encapsulation chip connect technologies, and multi-chip modules In these instances the defective chip is removed, the chip site redressed, and a new chip installed for **testing**. In the case of a polymeric substrate, redressing the chip site might include milling.

BSPR:
"High **Performance** Test System", IBM Technical Disclosure

Bulletin, Volume 33,
No. 1A (June 1990), pp 124-125, describes a test system for ULSI integrated
circuit memory and logic chips. In the described method, a first silicon **wafer**
"test board" has metallization complementary to the metallization of the second
silicon **wafer** to be tested. The second silicon **wafer** has C4 (controlled
collapse chip connection) Pb/Sn solder balls on the contacts. The first and
second silicon wafers have substantially flat and substantially parallel
surfaces, and are said to require a minimum of compressive force for **testing**.

BSPR:
"New Products Test **Interposer**" Research Disclosure, January 1990, Number 309
(Kenneth Mason Publications Ltd., England) describes a method for fabricating
an **interposer**-type test head to perform electrical **testing** of printed circuit
cards and boards prior to component assembly. The test **interposer** is built as
a mirror image circuit of the circuit to be tested. However, only the points
to be tested, as lands and pads, are present. Circuit lines are not present.
The test **interposer** pads are coated with a dendritic material to make
electrical contact to the corresponding points on the printed circuit component
to be tested. The circuit board or card and the tester are then brought into
contact for **testing**.

BSPR:
Compressive type testers are described generally in U.S. Pat. No. 4,716,124
to Yerman et al. for TAPE AUTOMATED MANUFACTURE OF POWER SEMICONDUCTOR DEVICES,
U.S. Pat. No. 4,820,976 to Brown for TEST FIXTURE CAPABLE OF ELECTRICALLY
TESTING AN INTEGRATED CIRCUIT DIE HAVING A PLANAR ARRAY OF CONTACTS, and U.S.
Pat. No. 4,189,825 to Robillard et al. for INTEGRATED TEST

AND ASSEMBLY
DEVICE.

BSPR:
The art has failed to provide a means for rapid, reproducible, low cost, high throughput **testing** of integrated circuit chips.

BSPR:
It is an object of the invention to provide a method and apparatus for rapid, reproducible, low cost, high throughput **testing** of integrated circuit chips.

BSPR:
It is a further object of the invention to provide a method and apparatus for rapid, reproducible, low cost, high throughput **testing** of integrated circuit chips that allows for easy chip positioning and temporary **attachment** and easy removal of chips after **testing,** particularly after burn-in **testing**.

BSPR:
The invention provides a method of **testing** semi-conductor chips. The integrated circuit chips are placed in a test fixture by a special tool, tested in the test fixture under carefully maintained test conditions, and removed without damage.

BSPR:
The invention further provides a chip test fixture system. This chip test fixture system utilizes a test carrier (also referred to herein as an "**interposer**") having contacts corresponding to the contacts on the semiconductor chip. The carrier contacts have, for example, dendritic surfaces. The chip contacts which may, for example, be C4 solder balls, solder bumps, brazing alloy bumps, metal pads or bumps, as gold, silver, copper, or aluminum bumps or pads, wire lead connection pads, or tape

automated bonding
connection pads, are brought into compressive contact with the carrier contacts
on the chip test fixture system. The compressive contact between the dendritic
surface and the chip contacts provides a highly electrically conductive
temporary bond. Test signal input vectors are applied to the inputs of the
semiconductor chip across these highly electrically conductive bonds, and
output signal vectors are recovered from the semiconductor chip across these
highly conductive bonds.

BSPR:
The chip tester of the present invention substantially reduces the need for
expensive rework. According to the method of the invention, there is provided
a method of **testing** semi-conductor chips. The individual semiconductor chips
have I/O, power, and ground contacts. In the method of the invention a test
fixture system is provided. The test fixture system includes a dedicated
fixture just for **testing chips,** a chip insertion tool, a chip positioning tool,
and a chip removal tool. The functions of the individual tools, that is, the
chip insertion tool, the chip positioning tool, and the chip removal tool, may
be combined into a smaller set of tools. This chip test fixture system has
contacts corresponding to the contacts on the semiconductor chip. The carrier
contacts are low electrical contact resistance contacts adapted for holding the
integrated circuit chip in place during **testing,** with low impedance, while
allowing easy removal of the chips after **testing**.

BSPR:
The chip contacts are brought into electrically conductive contact with the
dendrite bearing contacts on the test carrier. A good electrically conductive

contact must be a low impedance, low contact resistance contact, and the integrated circuit chip should be secured from lateral movement with respect to the substrate or fixture. Test signal input vectors are applied to the inputs of the semiconductor chip, and output signal vectors are recovered from the semiconductor chip. In the preferred embodiment of the invention, chip **testing** may be accelerated by heating the integrated circuit semiconductor chip or chips under test.

BSPR:
After **testing,** the temporary bonds are broken without damage to the chip or chip contacts, and the chip is carefully removed from the test fixture and if faulty are discarded and if good permanently **attached** to a suitable substrate.

DEPR:
According to the method of the invention, there is provided a method of **testing** semiconductor chips. herein, "**testing**" includes elevated temperature **testing,** i.e., burn in, as well as ambient **testing**. In a preferred embodiment of the invention, there is provided apparatus for placing semiconductor chips in the test fixture system, positioning and holding the semi-conductor chips before and during **testing,** and removing the semiconductor chips after **testing**. The individual semiconductor chips have I/O, contacts. In the method of the invention a chip test fixture system is provided. The test fixture system includes a burn in board or **interposer** with contacts which are aligned with the chip contacts, a means for placing the integrated circuit chips on the burn in board, a means for applying heat, a means for applying compressive force to the integrated circuit chips under test to form a good electrical contact between

the chip contacts and the **interposer** contacts, and a means for removing the
integrated circuit chips from the burn in board after completion of the test.

DEPR:
The chip contacts are brought into electrically conductive contact with the
conductor contacts on the burn in board of the test system. In the case of
flip chip connector chips, the chips are tested in their normal, contact down,
configuration. Chips intended for other mounting technologies, with their
contacts facing up, as tape automated bonding chips or wire lead connector
chips, can also be mounted for **testing** in an inverted configuration, with their
contacts facing downward. Test signal input vectors are applied to the inputs
of the semiconductor chip, and output signal vectors are recovered from the
semiconductor chip.

DEPR:
After **testing** the chip may be removed from the substrate.

DEPR:
According to a preferred exemplification of the invention there is provided a
method and apparatus for **testing** an integrated circuit semi-conductor chip.
The chip has a first plurality of I/O contacts providing signal, power, and
ground contacts. These contacts are typically chosen from the group consisting
of solder, low melting point alloys having a melting point below 200 degrees
Celsius, brazing alloys, or other conductive metals as gold, silver, copper, or
aluminum, They may be in the form of solder bumps or balls, controlled collapse
chip connector (C4) balls, and pads for wire lead bonding and tape automated
bonding. Generally, the chip contacts are characterized as being a structure
formed of a metallic material in which electrical contact

resistance is reduced
by abrasion or penetration by the tester contact.

DEPR:
The process of the invention starts by providing an integrated circuit chip
test system having a special and unique burn in board or **interposer** card
between a tester and the chip being tested. The board or card has a plurality
of contacts corresponding to the plurality of contacts on the chip to be
tested. The contacts on the burn in board are coupled to the tester and are
provided with high surface area conductor surfaces. Exemplary are columnar
dendrites of porous, columnar Pd atop a smooth Pd film.

DEPR:
The system may, and preferably does, include one or more heating systems. For
example, a resistance heater can be integral to and incorporated into the burn
in board, as well as heating elements in the compressive means. These heating
systems heat the semi-conductor chips under test. Heating the semiconductor
integrated circuit chip under test accelerates incipient failures and also
accelerates the **testing** process.

DEPR:
After **testing the chips** that have passed are separated from chips that have
failed. According to a further embodiment of the invention, "fast" chips can
be separated from "slow" chips.

DEPR:
It is, of course, to be understood that the heating assembly, the subsystem for
inserting the integrated circuit chips, and the subsystem for removing the
integrated circuit chips at the conclusion of **testing** can be one unit, fixture,
tool, or element.

DEPR:
FIG. 3 is a schematic flow chart of the method of the invention, showing an overview of both the general system and the process. An initially unpopulated burn in board 11 is populated with integrated circuit chips 31 by placing the chip contacts in contact with the burn in board contacts and heated by a heating assembly 51 applied over the integrated circuit chips 31 on the burn in board 11. The integrated circuit chips 31 are then tested electrically, logically, and thermally, as described hereinbelow. After **testing** the heating element 51 is removed from the integrated circuit chips 31 and the burn in board 11 and the integrated circuit chips 31 are separated therefrom and divided into defective chips and chips for placement on a printed circuit board, card, or other substrate.

DEPR:
The **testing** process requires initial high pressure to break through oxide films on the contact surfaces and effect a low electrical resistance contact, as well as sustained high pressure to avoid oxide formation and loss of electrical contact surface area, thereby reducing contact resistance and providing good electrical interconnection between the burn in board 11 and the integrated circuit chips 31 under test. Moreover, it is essential that the integrated circuit chip be held in place with a predetermined and controllable force, for example a chip specific force, a test fixture specific force, or a test procedure specific force. Chip specific forces are determined by the number and type of input/output (I/O) contacts on the integrated circuit chip being tested. Generally it has been found, that when solder balls and the like are to contact the above described dendrites, an applied force

of between 10 and 50 grams per chip contact provides satisfactory results. This translates in to a force of about 30 pounds per square inch for a chip having 350 contacts and 110 pounds per square inch for a chip having 1900 to 2000 contacts. When the chip is only provided with wire bond pads the required applied force may be reduced to between 5 to 25 grams per pad and still achieve satisfactory results.

DEPR:
Thus it is necessary to apply force to the load bearing surfaces opposite the electrical contact surfaces of the integrated circuit chips 31 to both achieve good electrical contact between the burn in board contacts 13 and the chip contacts 16 before **testing** and to retain this good contact between the board contacts 13 and the chip contacts 16 during **testing**. This can be accomplished an integrated chip retention fixture. One such fixture is shown in FIGS. 7A and 7B, while another such fixture is shown in FIGS. 8A and 8B.

DEPR:
Because, as noted above, the **testing** process requires initial high pressure to break through oxide films on the surface of the solder balls and contacts, as well as sustained high pressure to reduce contact resistance and provide good electrical interconnection between the burn in board and the integrated circuit chip, there may be adhesion of the integrated circuit chips 31 under test to the burn in board. Moreover, during **testing** thermal energy is both generated within the individual integrated circuit chips 31 and applied to the chips. This can, and frequently does, result in adhesion and even bonding of contacts between the individual integrated circuit chips 31 and the burn in board 11.

In order to avoid damaging the individual integrated circuit chips 31, especially after the application of sufficient force thereto to break any oxide films on the surface of the solder balls or other interconnects, and the continued application of mechanical force, electrical energy, and heat, it is frequently necessary to use a special tool to remove the integrated circuit chips 31 from the burn in board 11.

DEPR:
Generally, in the **testing** process the integrated circuit chip is powered, e.g., between inputs of V.sub.DD or V.sub.CC, and ground, and subjected to various logic and memory tests and to thermal loads. After **testing** the heating element 51, the chips 31 and the burn in board 11 are all separated. The individual integrated circuit chips are separated into defective chips, which are discarded and chips for placement on a printed circuit board, card, or other substrate.

DEPR:
As noted hereinabove, the **testing** process subjects the integrated circuit chip to compressive and thermal loads which, while necessary to break through oxide films on the surface of the solder balls and contacts, reduce contact resistance, and provide good electrical interconnection between the burn in board 11 and the integrated circuit chip 31, which can, and frequently do, result in adhesion and even bonding of contacts between the individual integrated circuit chips 31 and the burn in board 11. Thus, to avoid damaging the individual integrated circuit chips 31, it is may be necessary to use high pressure and vacuum tools to remove the integrated circuit chips 31 from the burn in board 11.

DEPR:
Passive pattern sensitive faults are tested for by setting the contents of the
adjacent memory cells, A,B,C,D from [0,1], and setting the base cell, E, to
E=.uparw. and E=.dwnarw., and reading the base cell, E. For a passive pattern
sensitive fault, we expect the measured value of the contents of cell E to be a
function of the contents of the surrounding cells, and not necessarily the
value set by the **testing** program.

DEPR:
In **testing** for active pattern sensitive faults, we place fixed values in three
of the four neighboring cells (i.e., three of the four cells, A,B,C, and D),
and the base cell. We then transition the remaining neighbor cell, and see if
this changes the contents of the base cell, E.

DEPR:
Testing for passive pattern sensitive faults requires .about.65n tests, where n
is the number of cells. **Testing** for active pattern sensitive faults requires
.about.100n tests, where n is the number of cells.

DEPR:
Turning now to FIGS. 15-24, further embodiments and variations of the chip
insertion, placement and hold down compression fixture suitable for holding a
chip on a burn in board or **interposer** card will be described. When an
interposer card or test carrier is used it is provided with suitable contact
means such as extended pins, leads or land grid arrays such that it can be
plugged into a burn in board or a test head. In the present embodiment it will
be assumed that an **interposer** card is used and that it will, during the actual
test procedure, be plugged into a separate burn in board and the unified burn

in board and the hold down compression fixture will be inserted in a suitable heating and **testing** oven. Such ovens are commercially available and well known to the art.

DEPR:
Referring to FIGS. 15 to 17, the alternate embodiment includes an upper heat sink 200 affixed by a plurality of screws 201 to a lower heat sink 202 securing therebetween a body cover 203, provided with a gimbal screw 204 which is in turn locked into a body fixture 205 carrying a chip 230 positioned on a burn in board or **interposer** 206.

DEPR:
The body fixture 205, shown in section and in greater detail in FIG. 18A, is generally square and has a circular central opening 207 having on its interior surface a plurality of beveled locking recesses 208 one of which is provided with a stop 209 in the form of a pin extending across one of the beveled recesses 208. The beveled locking recesses 208 are separated by receiving recesses 208a (FIG. 17). Located below the main portion of the body fixture there are, on three sides thereof, suspended a plurality of supports 210 for locating and, in conjunction with a locking plate 211 located on the fourth side thereof, holding the **interposer** 206 in a fixed position. The locking plate 211 is held on the fourth side of the body 205 by suitable screws 212.
In FIG. 18B a variation of holding the **interposer** 206 in a fixed position is shown and comprises four locking plates 213 held on to the bottom 214 of the body fixture 205 by a series of screws 215.

DEPR:
Referring to FIG. 21, the body cover 203 is generally in the form of a spoked

wheel with a rim 225 supported by four spokes 226 forming an X. The rim 225 has an outer diameter that will fit within the opening 207 in the lower body fixture 205 and an inner diameter slightly larger than the outer diameter of the lower heat sink 202. In the center of the spokes 226 which there is a central, threaded opening 227 in which the gimbal screw 204 is positioned. In this embodiment this gimbal screw is preferably made out of a compatible non-oxidizing material capable of supplying a suitable force at temperatures encountered in burn-in **testing,** e.g., 120.degree.-180.degree. C. On the outside of the rim 225 and in line with each of the four spokes are extended locking ears 228. In two of the spokes there is provided locating holes 221a which mate with the positioning pins 221 in the lower heat sink 202.

DEPR:
To assemble the unit the body cover 203 is placed over the lower heat sink 202 so that the lower heat sink fits within the rim 225 and the spokes 226 fit into the channels 220 with the pins 221 being aligned with the hole 221a in the body cover spokes 226. When the body cover is properly aligned with the lower heat sink the upper mesas 219 loosely pass through corresponding openings 231 in the body cover 203. Since each of these lands 219 are provided with screw holes 201a the upper heat sink 200 is **attached** to the lower heat sink 202 by the screws 201. It should be noted that the body cover spokes 226 are slightly smaller, i.e., thinner in both height and width, than the lower heat sink channels 220 and thus the lands 219, of the lower heat sink extend above the upper surface of the body cover 203. Thus, when the heat sinks are secured together, the body cover is only loosely held therebetween.

DEPR:
The body fixture 205 is now provided with an **interposer** 206 and a chip 230 is
placed thereon so that the contact pads on the chip are aligned with and are in
contact with the contacts on the **interposer** as described in conjunction with
FIG. 4. The heat sink body cover assembly, which includes the body cover 203
held therebetween, is now placed in the body fixture so that the body cover
fits within the opening 207 and the ears 228 on the outer rim of the body cover
fit into the recesses 208a. The heat sink body cover assembly is then turned
clockwise so that the ears 228 on the body cover pass in to the beveled locking
recess 208 until one of the ears abuts the pin 209. The fit between the ears
228 and the locking recesses 208a allows some play between the body cover 203
the body fixture 205. A circular wave spring 234 (FIG. 17) is positioned in
recess 208 and is staked in place with pin 209 so as to prevent rotation of the
spring. Spring 234 is sized and configured so that it contacts and biases
upwardly the bottom surface of ears 228 of body cover 203. The spring force of
wave spring 234 has a magnitude sufficient to drive body cover 203 upwardly
against the upper wall of recess 208 with a force sufficient to substantially
prevent lateral movement of cover 203 when the latter is loosened. In one
embodiment, a spring force of 2-5 lbs. was found to be satisfactory. Once the
body cover 203 is locked into the body fixture 205 it effectively becomes a
gimbal ring for the joined upper and lower heat sinks. The gimbal screw 204 is
now turned to force a ball bearing 204a (FIG. 16), located in its bottom
center, against the bearing plate 224 which in turn bears against and
compresses the flat spring 223 and forces the pedestal 202a

(FIGS. 16 and 20)
of the lower heat sink against the chip 230 further assuring that good
electrical contact is made between the chip contacts and the contacts on the
interposer 206. The gimbal screw 204, the ball bearing 204a, the bearing plate
224 and the flat spring 223 all co-act to assure that the fastened together
upper and lower heats sinks have, around the body cover, sufficient gimballing
action such that the bottom of pedestal 202a moves enough to become flat
against the back of the chip 230 and apply an even pressure across the entire
chip. This even pressure assures that a good electrical contact is made
between all the chip contacts and **interposer** contacts.

DEPR:
If the chip, under test is one that is provided with projecting contacts, such
as solder balls, when it becomes heated the projecting contacts may soften.
Such softening can, unless continuous pressure is maintained between the chip
contacts and the **interposer** contacts, cause the contacts to loosen with respect
to each other, with good electrical contact therebetween after being lost. The
flat spring 223 prevents such loosening and loss of electrical contact.
Because the spring is compressed by the gimbal screw when the contacts soften
or begin to loosen as result of heating, the spring begins to relax and expand
and thus forces the bearing plate up against the ball bearing and the lower
heat sink down against the chip. The compressed spring thus maintains adequate
force between the chip and **interposer** contacts such that good electrical
contact therebetween is maintained.

DEPR:
Once the chip is securely held in place by the gimbal screw being tightened

down, the entire fixture and **interposer** is placed in the tester 161 where appropriate test conditions are applied to the chip. When the tests are completed the fixture and **interposer** is removed from the tester and the chip removed from the fixture.

DEPR:
FIG. 23 shows an alternative embodiment of the gimbal screw 204 of FIG. 16. In this FIG. the gimbal screw 204 has an internal spring 240 contained in a central cavity 241. This spring 240 bears on a ball bearing 242 which in turn bears against a bearing plate 224 adapted for interacting with lower heat sink 202 and applying the continuous pressure needed to prevent change in the contacts during **testing** from interfering with the good electrical contact between the chip and the **interposer** contacts as described above in conjunction with FIGS. 15 to 22.

DEPR:
Leadless chips, i.e., those chip to be secured to a leadframe by wire bonding or TAB bonding, typically do not have solder balls or other contacts that extend any appreciable amount above the surface of the chip face, but rather have flat thin contact pads usually formed of aluminum or gold or the like. These leadless chips cannot be used with the **interposer** or burn in board arrangement as shown in FIG. 4. To contact such leadless chip the contacts on the **interposer** 246 must be provided with contacts that rise above its upper face so that a good electrical connection can be made to the chip contacts. Typically, such contacts are partially embedded in an insulator layer that prevents deformation, e.g., bending, of the contacts. Even if raised contacts are provided on the **interposer** surface, a leadless chip

placed on the
interposer can easily slip out of position if jostled prior to the heat sink
body cover assembly being placed thereon and the gimbal screw being tightened
down. To restrain the device from moving prior to clamping the chip on the
interposer by the gimbal screw, a temporary hold down mechanism is needed.

DEPR:
The fixtures described above and illustrated in FIGS. 15-24 are designed so
that the force applied to individual chip contacts (pads) fall within the range
described above relative to the fixtures illustrated in FIGS. 7A, 7B, 8A and
8B, i.e., 10-50 grams per contact when dendrites are used as the contacts on
interposer 206 and 5-25 grams per contact (pad) when wire contacts are used on
the **interposer**. Thus the fixtures described above and illustrated in FIGS.
15-24 are designed so that the force applied to individual chip contacts will
cover the entire range of 5 to 50 grams per contact.

DEPR:
FIG. 24 shows a vacuum based arrangement particularly adapted for temporarily
holding such leadless chips in place until the gimbal screw can be tightened
down on the chip. In particular FIG. 24 shows a sectional view of the body
fixture 205 with a modified **interposer** 246 positioned therein. This **interposer**
is provided with an opening 247 which is placed over and in line with a vacuum
port adapter 248. The vacuum adapter 248 is provided with a soft tip 249 that
makes a good seal with the bottom 246a of the **interposer** 246 and is coupled to
a suitable vacuum source (not shown). When a chip is placed on the **interposer**
246 a vacuum is drawn and the chip is held firmly until the heat sink body
cover assembly can be placed in the body fixture 205 and

the gimbal screw
tightened down. Once the gimbal screw is tightened down the vacuum is broken
and the entire compressive force fixture is removed from the vacuum adaptor
248. Although this vacuum adapter is particularly useful when handling
leadless chips it is also useful with any chip.

DEPV:
3. Sub-systems for placing the integrated circuit chip or chips on the burn in
board, and for removing the integrated circuits from the burn in board at the
conclusion of **testing**.

CLPR:
1. A chip to **interposer** aligning and clamping tool comprising:

CLPR:
2. The clamping tool of claim 1 wherein said means for temporarily holding
said chip on said **interposer** includes a hole passing through said **interposer**
beneath said specified position, and vacuum means coupled to said hole for
drawing a vacuum through said hole.

CLPV:
an **interposer** having a plurality of contacts thereon;

CLPV:
a body fixture for holding said **interposer** in a fixed position;

CLPV:
means for temporarily holding a chip having a plurality of contacts in a
specified chip position on the surface of said **interposer,** said plurality of
interposer contacts corresponding in number and position to said plurality of
chip contacts;

CLPV:
means for selectively clamping said chip on said **interposer**

in said position
with a compressive force selected from the range of between 5 and 50 grams for
each contact on said chip to electrically bond each of said chip contacts to a
corresponding one of said contacts on said **interposer**.